

CLAIMS

What is claimed is:

- 1 1. An integrated circuit package, comprising:
2 a substrate;
3 an integrated circuit mounted to said substrate;
4 a first underfill material attached to said
5 substrate and said integrated circuit; and,
6 a second underfill material that is attached to
7 said integrated circuit and said substrate.
- 1 2. The package as recited in claim 1, wherein
2 said second underfill material seals said first
3 underfill material.
- 1 3. The package a recited in claim 1, wherein said
2 first underfill material has an adhesion strength that
3 is greater than an adhesion strength of said second
4 underfill material.
- 1 4. The package as recited in claim 1, wherein
2 said first underfill material is an epoxy.

1 5. The package as recited in claim 4, wherein
2 said second underfill material is an anhydride epoxy.

1 6. The package as recited in claim 1, further
2 comprising a solder bump that is attached to said
3 integrated circuit and said substrate.

1 7. A process for underfilling an integrated
2 circuit that is mounted to a substrate, comprising:
3 dispensing a first underfill material which
4 becomes attached to the integrated circuit and the
5 substrate; and,
6 dispensing a second underfill material which
7 become attached to the integrated circuit and the
8 substrate.

1 8. The process as recited in claim 7, wherein the
2 first underfill material flows between the integrated
3 circuit and the substrate.

1 9. A process as recited in claim 8, wherein the
2 substrate moves within an oven while the first
3 underfill material flows between the integrated circuit
4 and the substrate.

1 10. The process as recited in claim 7, wherein the
2 second underfill material is dispensed in a pattern
3 which surrounds the first underfill material.

1 11. The process as recited in claim 7, further
2 comprising the step of heating the substrate before the
3 first underfill material is dispensed.

1 12. The process as recited in claim 11, further
2 comprising the step of heating the first underfill
3 material to a partial gel state.

1 13. The process as recited in claim 12, wherein
2 the substrate is heated to a temperature that is
3 greater than a temperature of said partially gelled
4 first underfill material.

1 14. The process as recited in claim 7, further
2 comprising the step of mounting the integrated circuit
3 to the substrate with a solder bump before the first
4 underfill material is dispensed.

1 15. A process for mounting and underfilling an
2 integrated circuit to a substrate, comprising:

3 baking the substrate;
4 mounting an integrated circuit to the substrate;
5 dispensing a first underfill material onto the
6 substrate, wherein the first underfill material flows
7 between the integrated circuit and the substrate while
8 the substrate moves through an oven; and,
9 dispensing a second underfill material around the
10 first underfill material.

1 16. The process as recited in claim 15, further
2 comprising the step of mounting the integrated circuit
3 to the substrate with a solder bump before the first
4 underfill material is dispensed.